What is claimed is:

1. A semiconductor integrated circuit device comprising an MIM structure capacitor connected between a power source potential electrode wiring and a ground potential electrode wiring each via at least one interlayer connection wiring.

2. The semiconductor integrated circuit device according to claim 1, wherein a metal electrode on one side of said MIM structure capacitor is connected to said power source potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

3. The semiconductor integrated circuit device according to claim 2, wherein a metal electrode on the other side of said MIM structure capacitor is connected to said ground potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

4. The semiconductor integrated circuit device according to claim 1, wherein said power source potential electrode wiring and said ground potential electrode wiring are adjacent to each other via an insulation film.

5. The semiconductor integrated circuit device according to claim 1, wherein said power source potential electrode wiring is a power source potential electrode pad to which a power source potential is supplied and an external wiring is connected, and said ground potential electrode wiring is a ground potential electrode pad which is grounded and to which an external wiring is connected.

6. The semiconductor integrated circuit device according to claim 1, where said power source potential electrode wiring is a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit

body and to which a power source potential is supplied, and said ground potential electrode wiring is a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

7. A semiconductor integrated circuit device comprising:

a metal electrode on one side connected to a power source potential electrode wiring via at least one interlayer connection wiring;

a metal electrode on the other side connected to a ground potential electrode wiring via at least one interlayer connection wiring; and

an insulation dielectric sandwiched by said metal electrode on one side and said metal electrode on the other side.

8. The semiconductor integrated circuit device according to claim 7, wherein said metal electrode on one side is connected to said power source potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

9. The semiconductor integrated circuit device according to claim 7, wherein said metal electrode on the other side is connected to said ground potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

10. The semiconductor integrated circuit device according to claim 7, wherein said power source potential electrode wiring and said ground potential electrode wiring are adjacent to each other via an insulation film.

11. The semiconductor integrated circuit device according to claim 7, wherein said power source potential electrode wiring is a power source potential electrode pad to which a power source potential is supplied and an external wiring is connected, and said ground potential electrode wiring is a ground potential electrode pad which is grounded and to which an external wiring

is connected.

12. The semiconductor integrated circuit device according to claim 7, wherein said power source potential electrode wiring is a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring is a loop-shape ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

13. A method of manufacturing a semiconductor integrated circuit device comprising:

forming an MIM structure capacitor;

covering said MIM structure capacitor with an interlayer insulation film;

opening contact holes in said interlayer insulation film on a metal electrode on one side and a metal electrode on the other side of said MIM structure capacitor;

forming an interlayer connection wiring in said contact holes; and

forming a power source potential electrode wiring and a ground potential electrode wiring connected to said metal electrode on one side and said metal electrode on the other side, respectively, each via said interlayer connection wiring.

14. The method of manufacturing a semiconductor integrated circuit device according to claim 13, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said power source potential electrode wiring and said metal electrode on one side.

15. The method of manufacturing a semiconductor integrated circuit device according to claim 13, further forming two or more interlayer connection wirings including said interlayer

connection wiring and at least one metal wiring layer between said ground potential electrode wiring and said metal electrode on the other side.

16. The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said power source potential electrode wiring and said ground potential electrode wiring are formed so as to be adjacent to each other via an insulation film.

17. The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said power source potential electrode wiring is formed as a power source potential electrode pad to which a power source potential is supplied and an external wiring is connected, and said ground potential electrode wiring is formed as a ground potential electrode pad which is grounded and to which an external wiring is connected.

18. The method of manufacturing a semiconductor integrated circuit device according to claim 13, where said power source potential electrode wiring is formed as a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring is formed as a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

19. A method of manufacturing a semiconductor integrated circuit device comprising:

forming a metal electrode on one side;

forming an insulation dielectric on a part of said metal electrode on one side;

forming a metal electrode on the other side on said insulation dielectric;

covering said metal electrode on one side, said metal

electrode on the other side, and said insulation dielectric with an interlayer insulation film;

opening contact holes in said interlayer insulation film on said metal electrode on one side and said metal electrode on the other side;

forming an interlayer connection wiring in said contact holes; and

forming a power source potential electrode wiring and a ground potential electrode wiring connected to said metal electrode on one side and said metal electrode on the other side, respectively, each via said interlayer connection wiring.

20. The method of manufacturing a semiconductor integrated circuit device according to claim 19, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said power source potential electrode wiring and said metal electrode on one side.

21. The method of manufacturing a semiconductor integrated circuit device according to claim 19, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said ground potential electrode wiring and said metal electrode on the other side.

22. The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring and said ground potential electrode wiring are formed so as to be adjacent to each other via an insulation film.

23. The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring is formed as a power source potential electrode pad to which a power source potential is supplied and

an external wiring is connected, and said ground potential electrode wiring is formed as a ground potential electrode pad which is grounded and to which an external wiring is connected.

24. The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring is formed as a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring is formed as a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.